

Do not enter

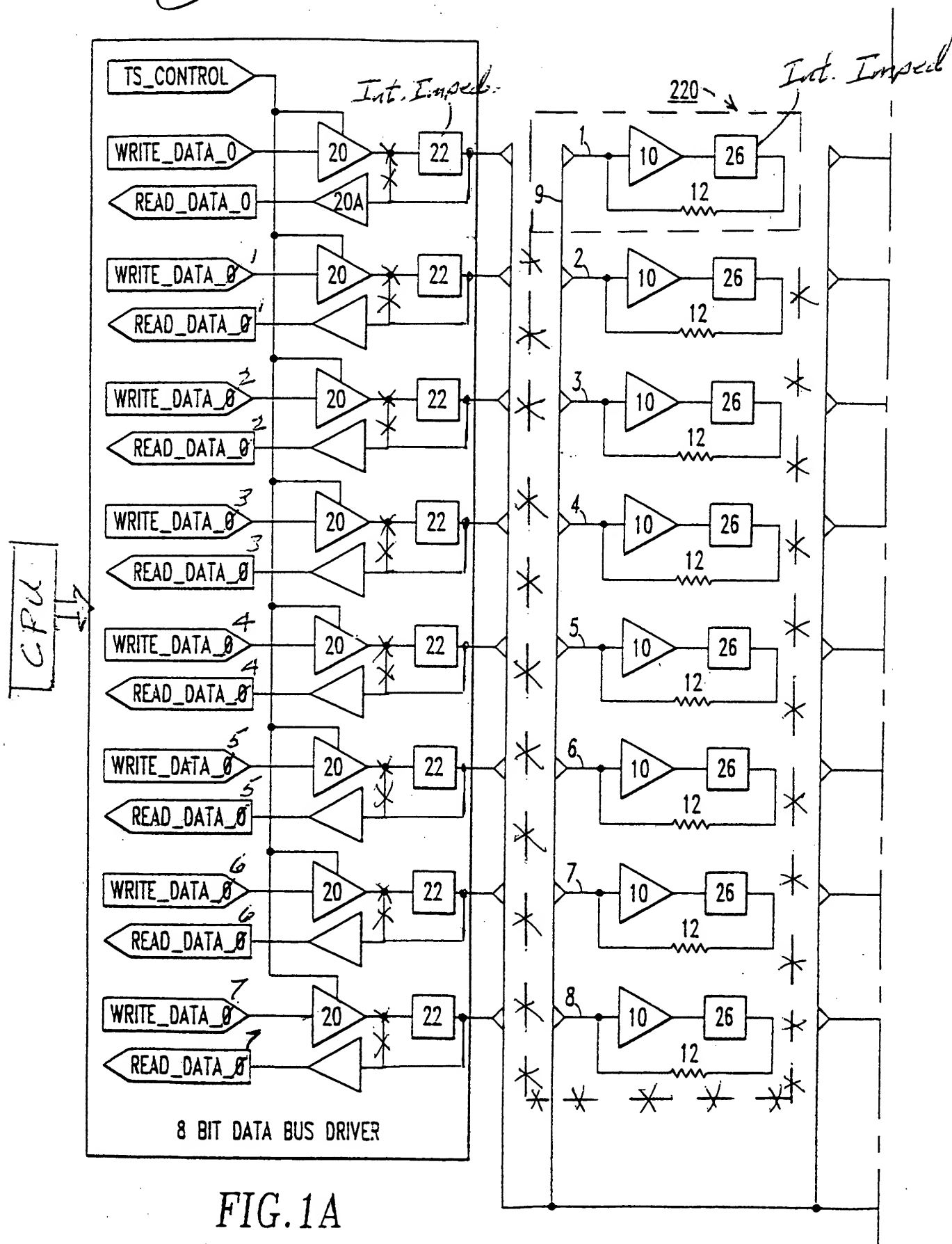
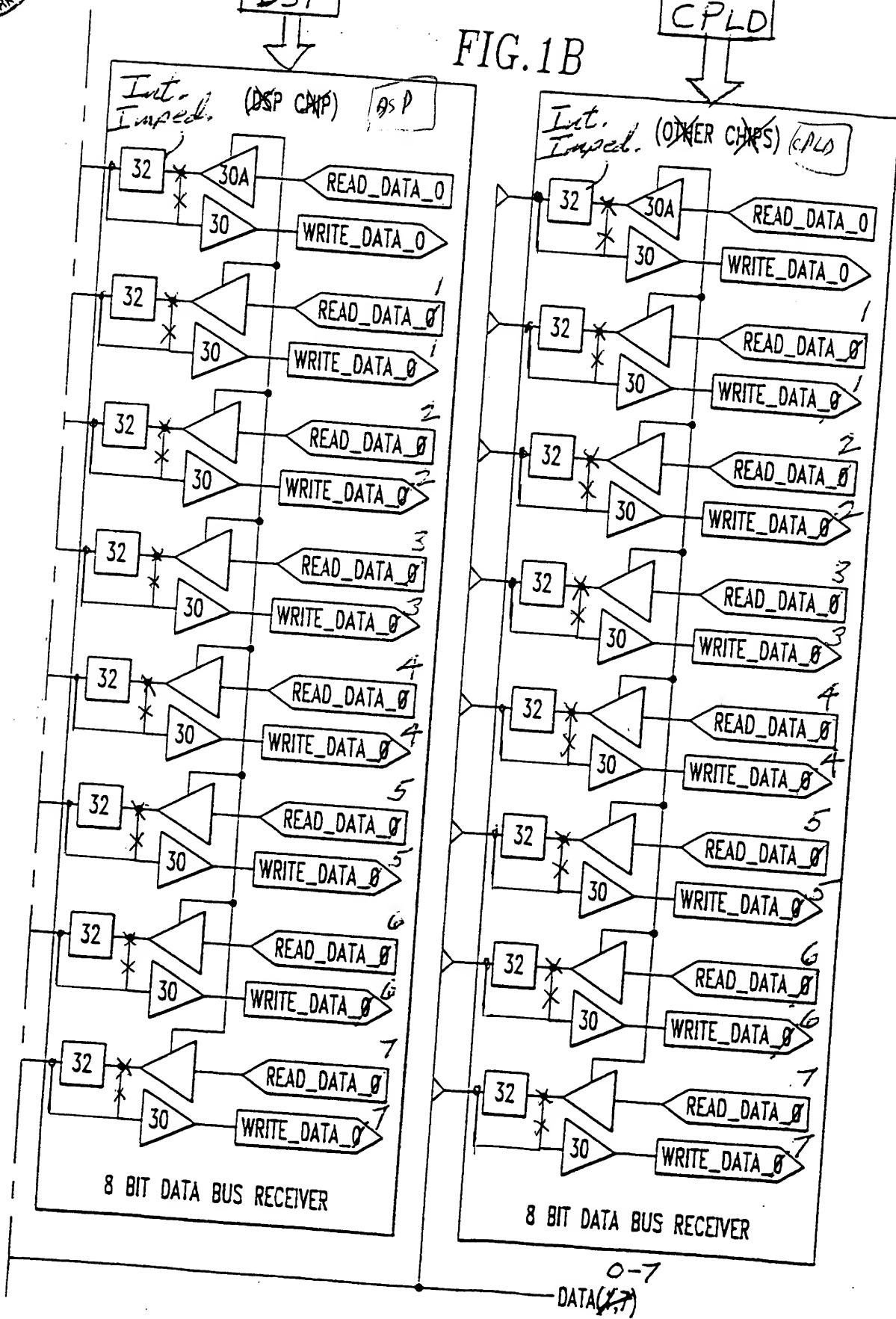


FIG.1A

DSP

FIG. 1B

CPLD



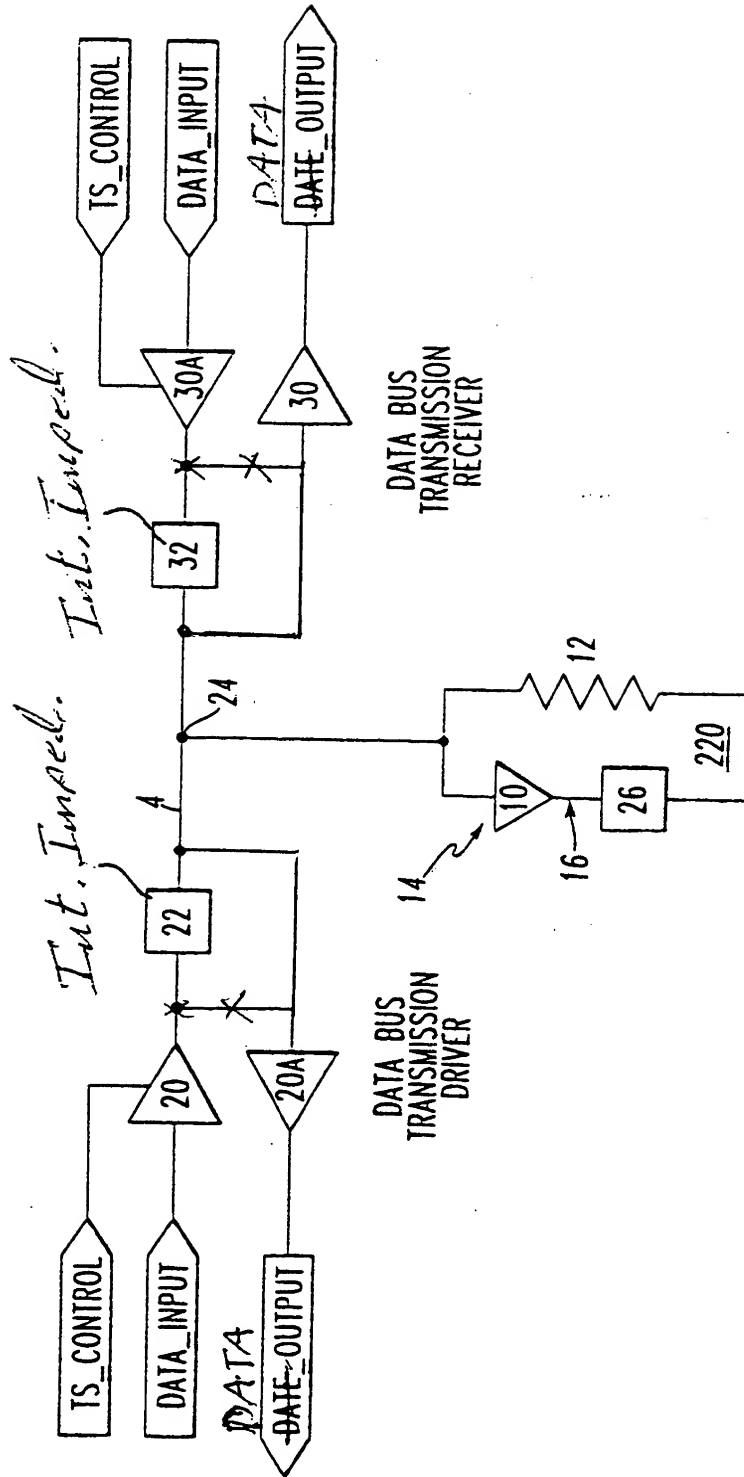
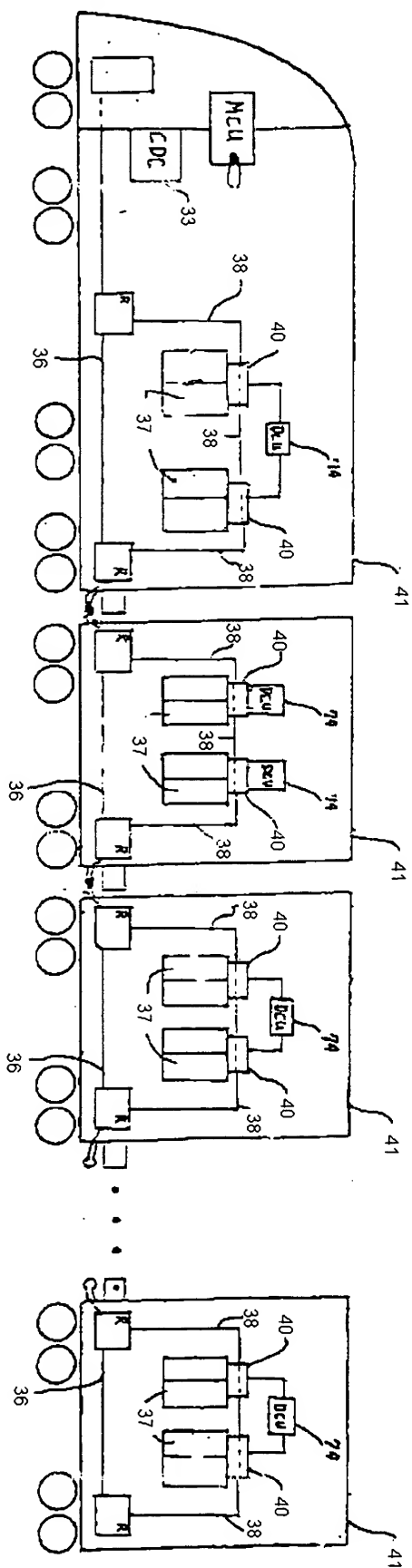


FIG.2

FIGURE 3A
(Prior Art)



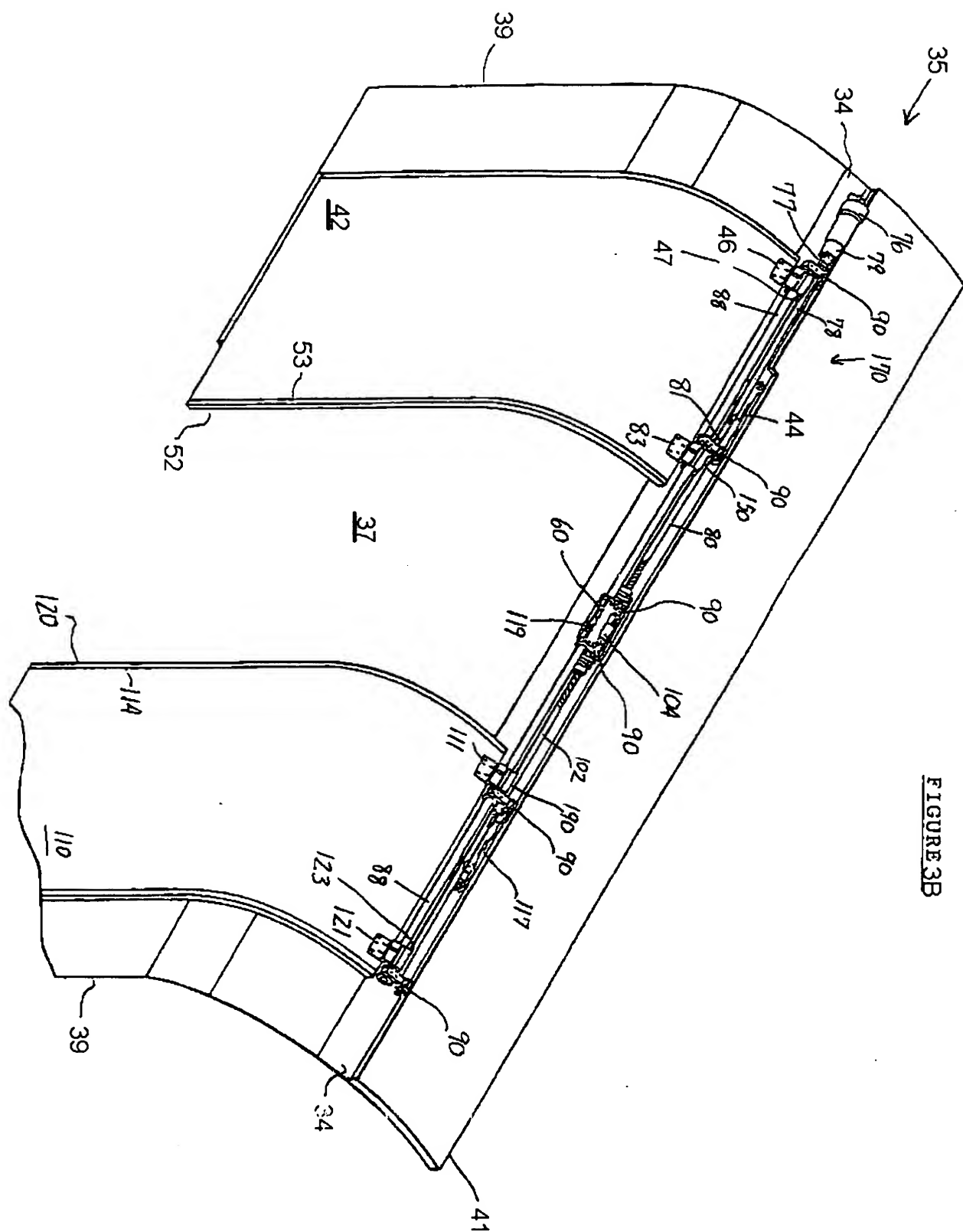


FIGURE 3B

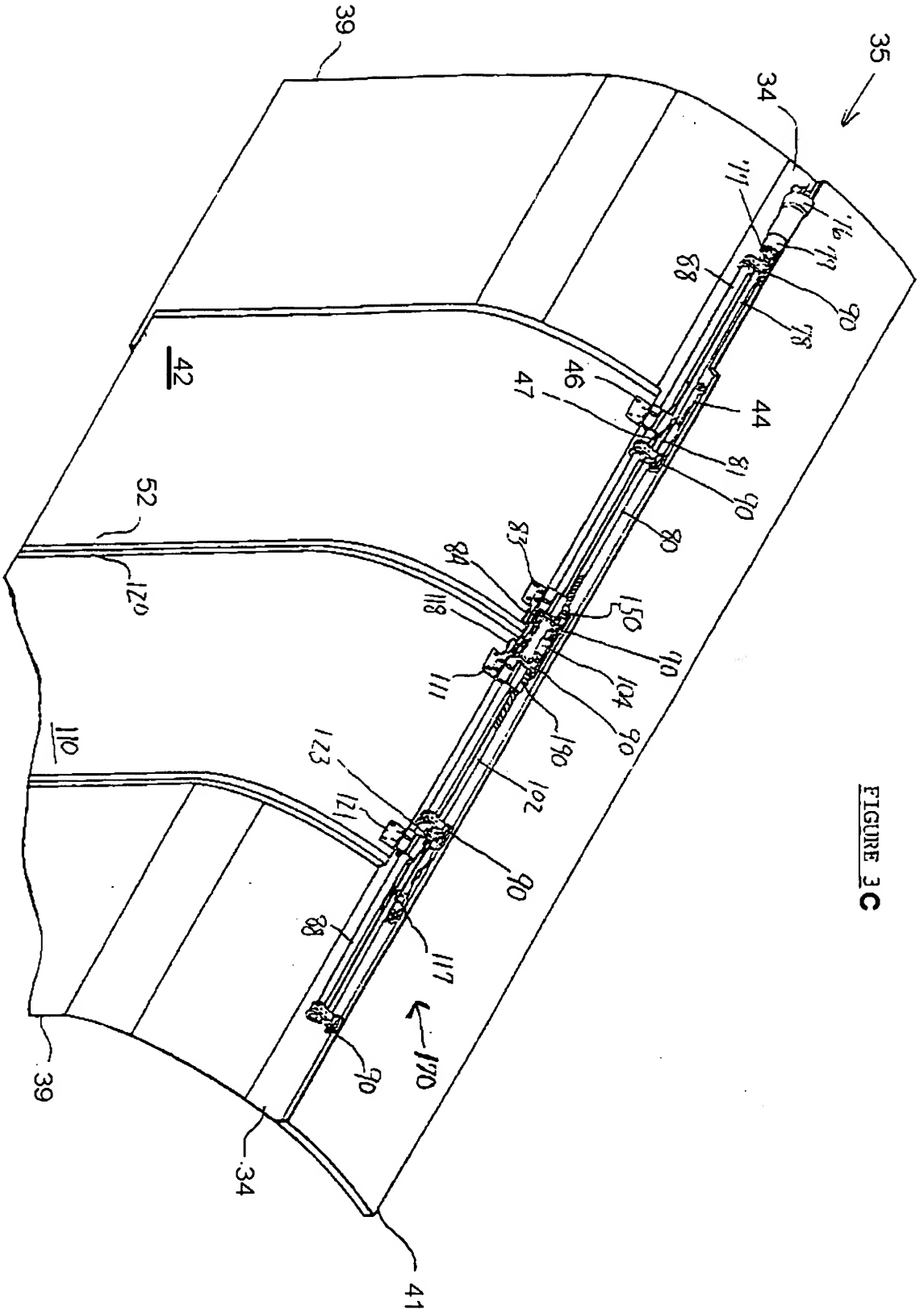


FIGURE 3C

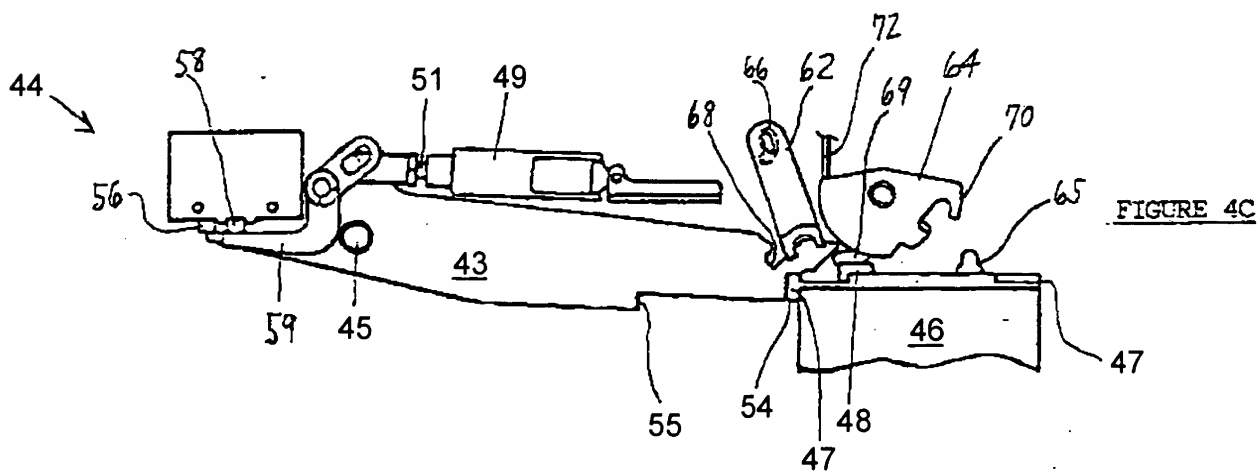
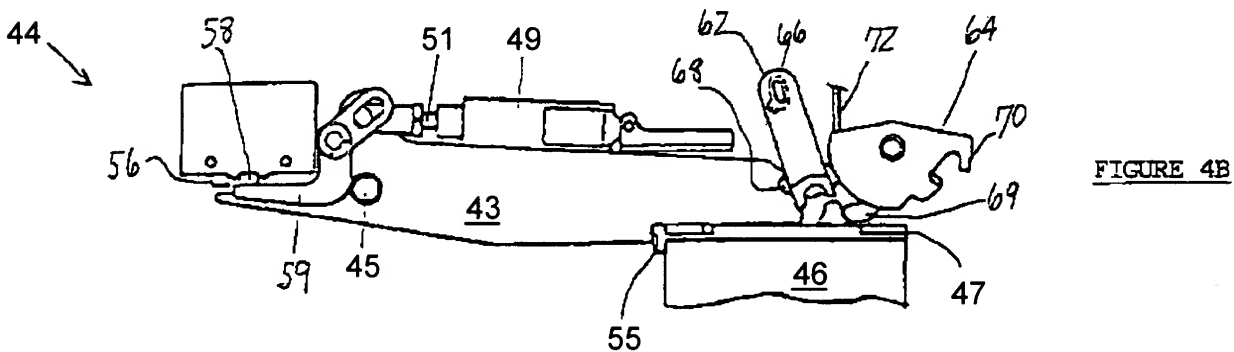
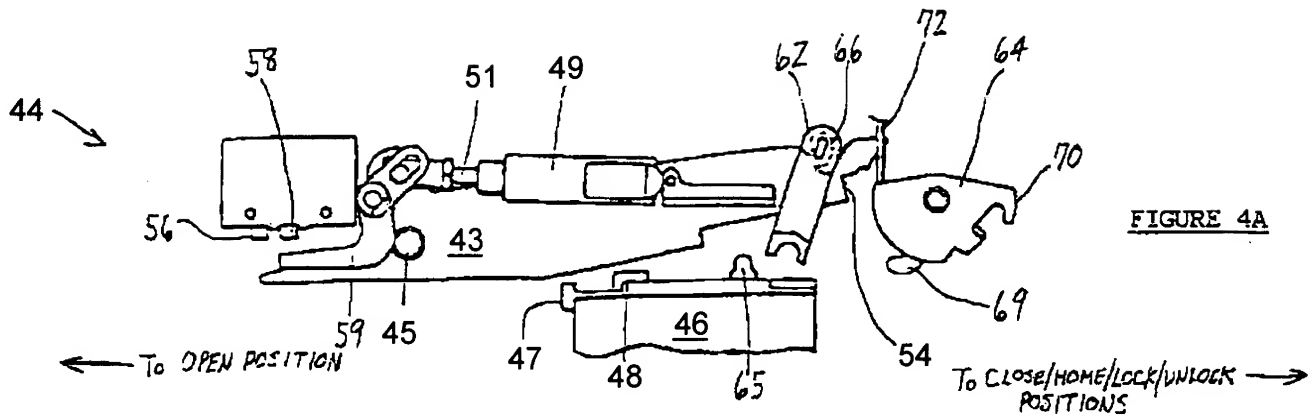


FIGURE 5A

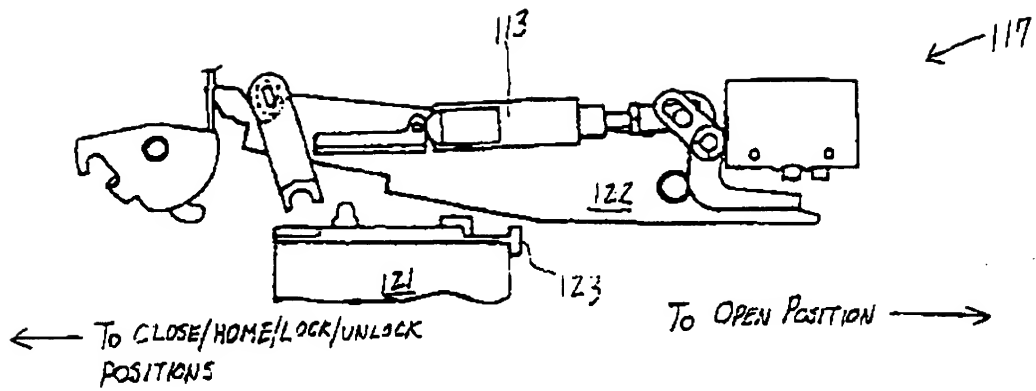


FIGURE 5B

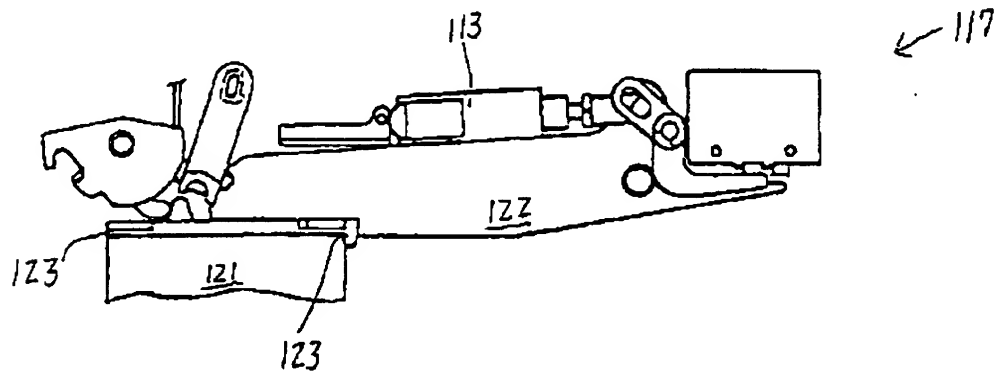


FIGURE 5C

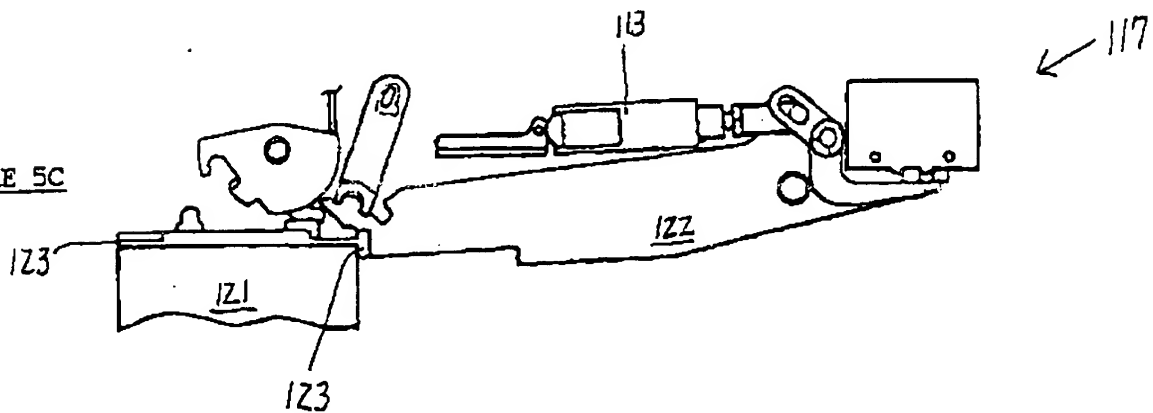
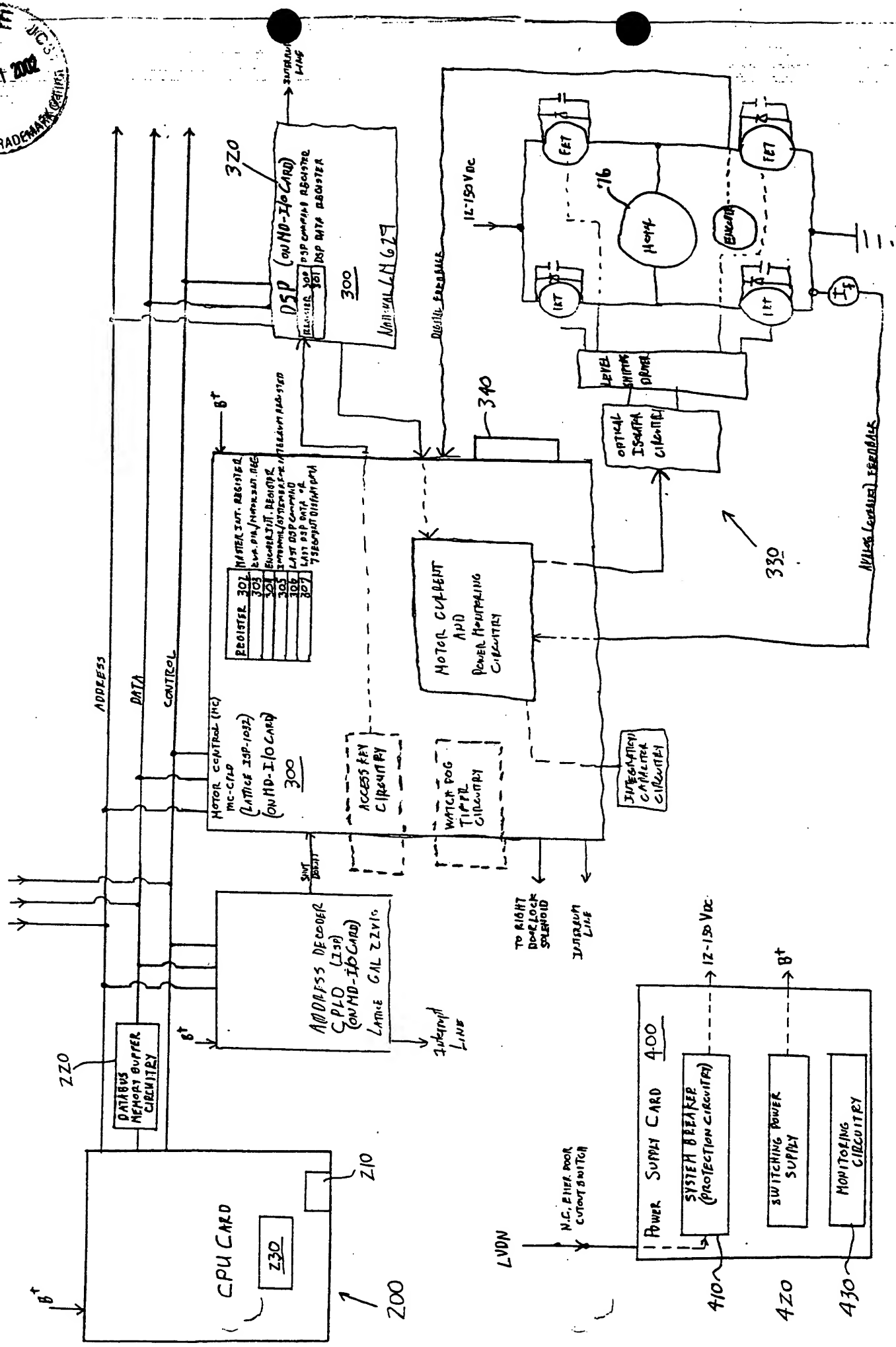




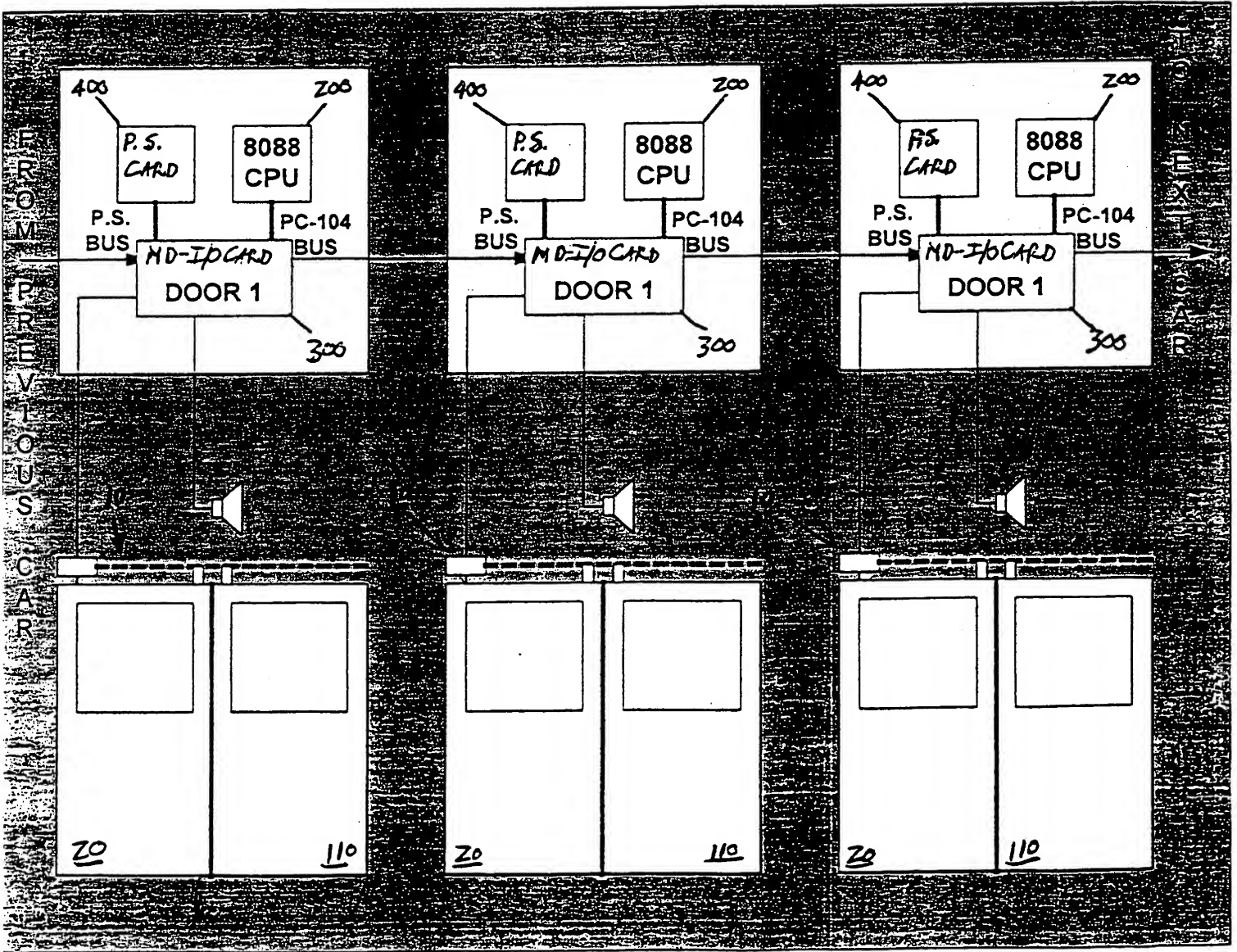


FIGURE 7B



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FIGURE 8



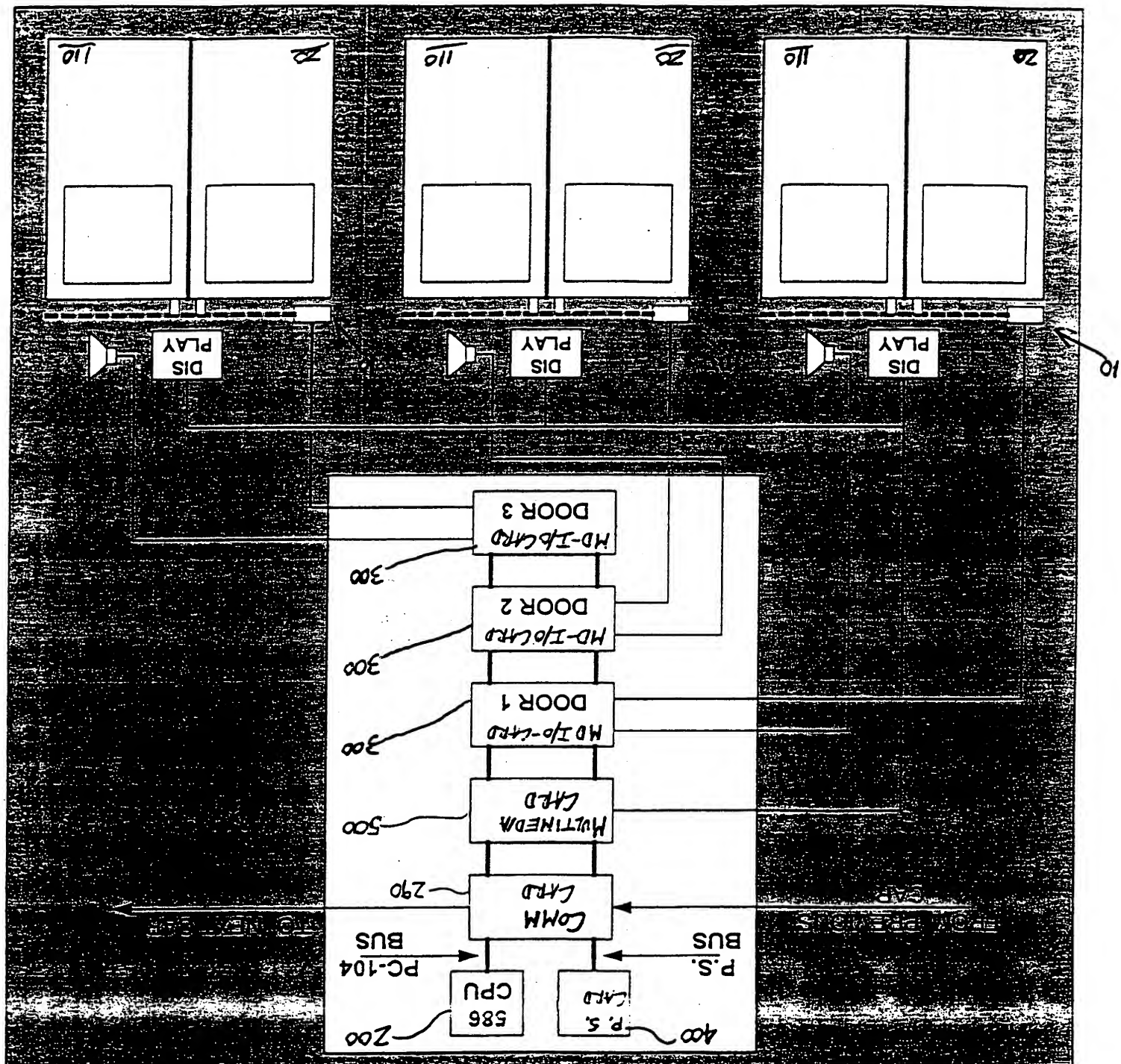
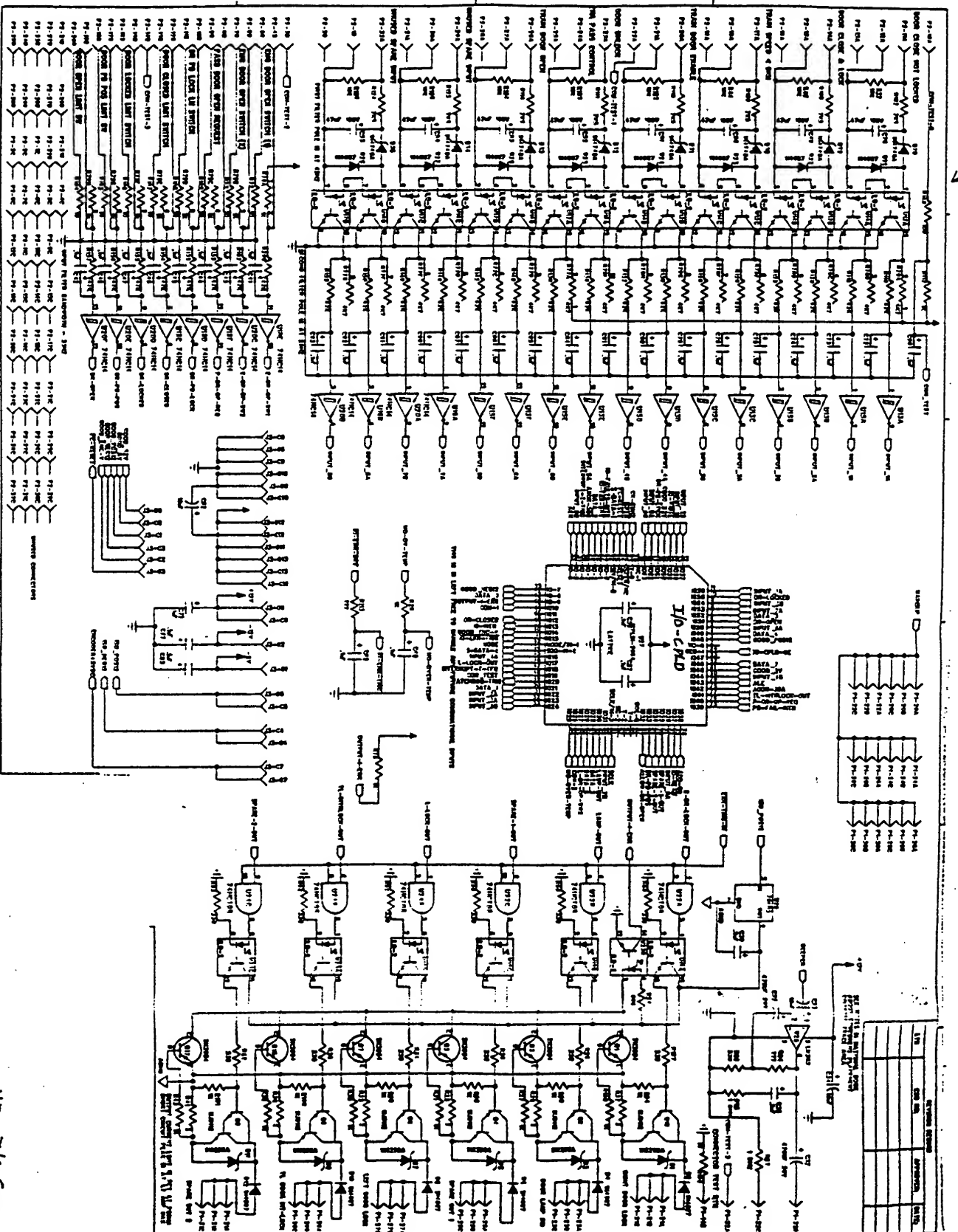


FIGURE 9

FIGURE 10A



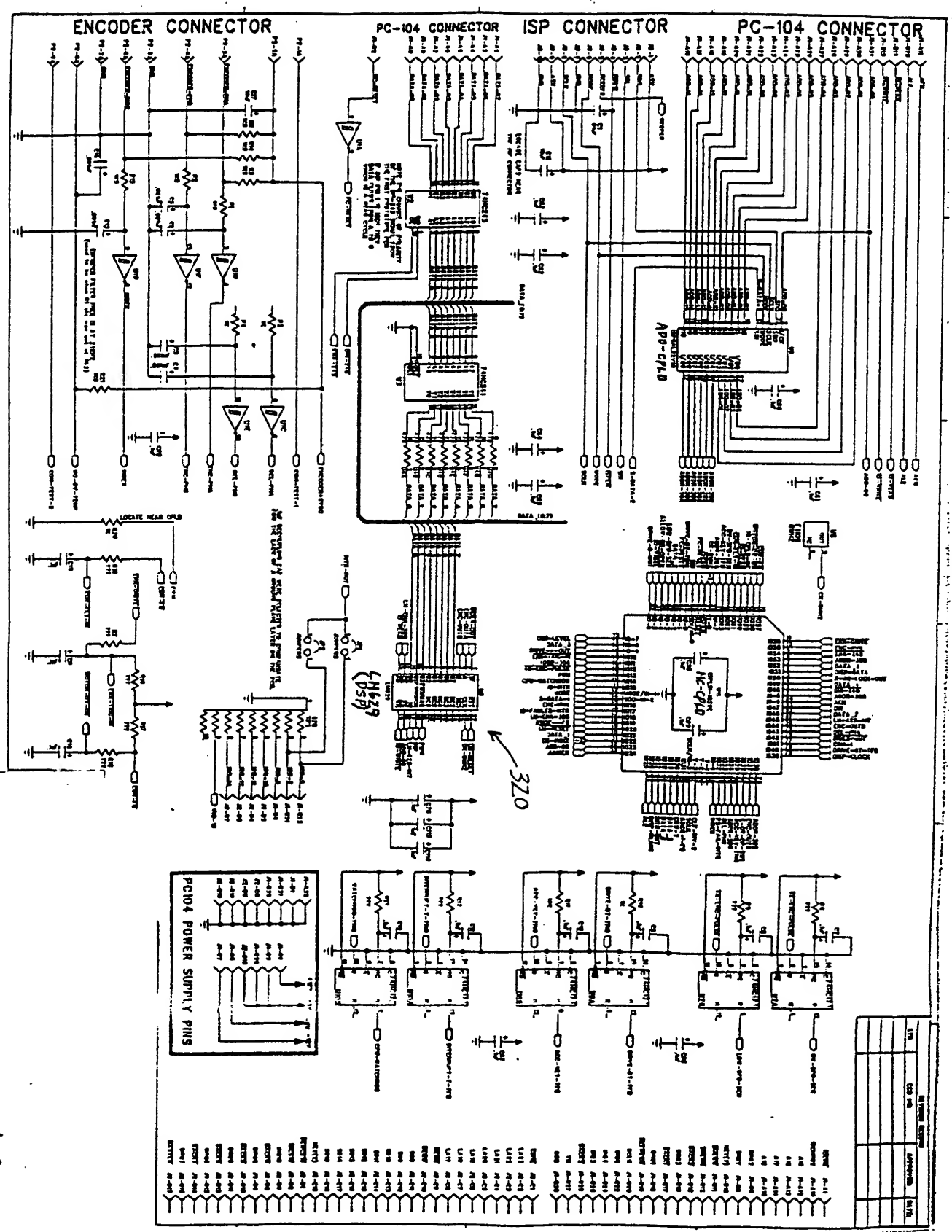
MD-I/O CARD

LAYOUT 1

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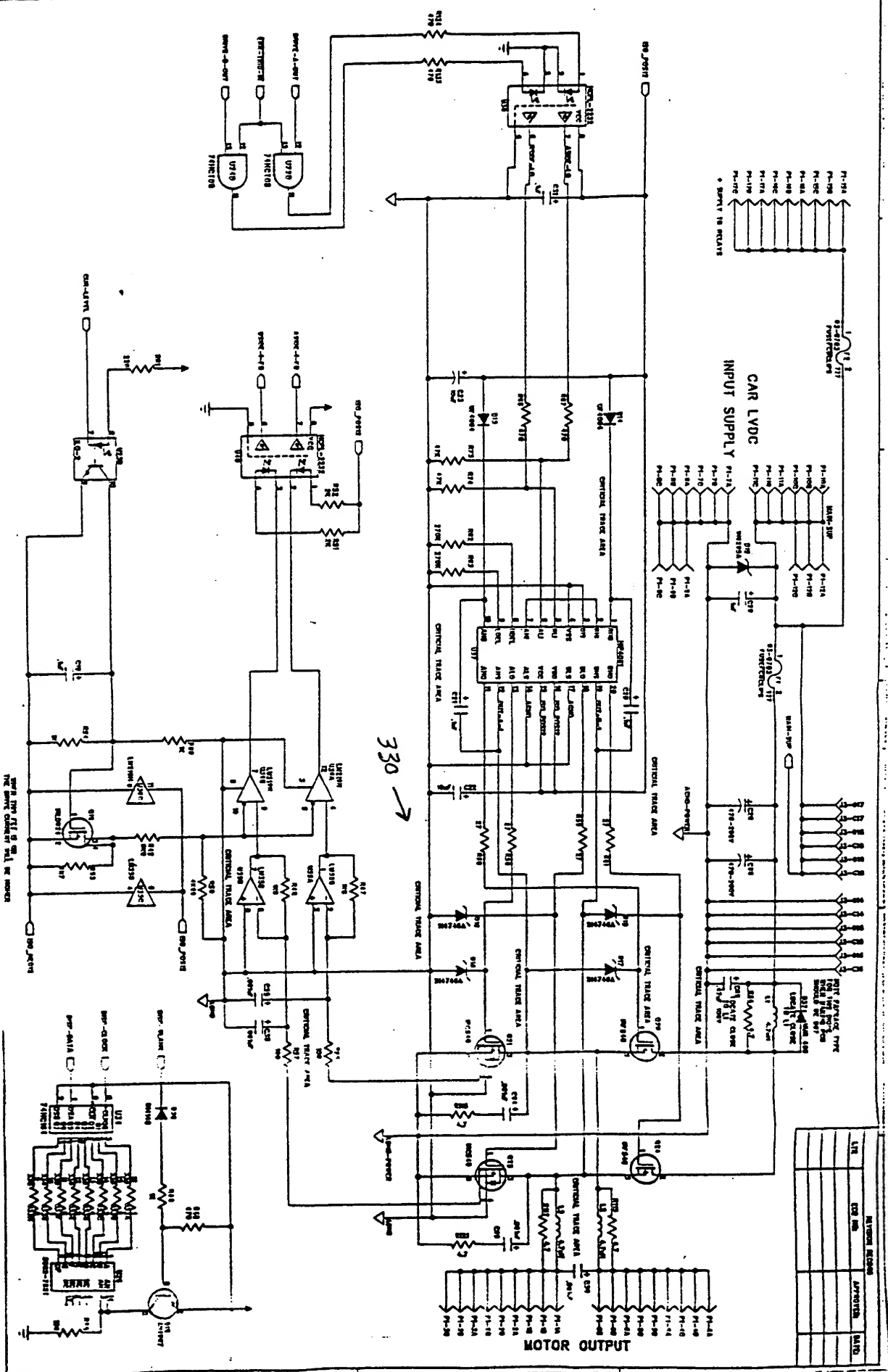
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FIGURE 10B



MD-IPb CARD
LAYOUT Z

FIGURE 10C



MD-I/O CARD
Layout 3

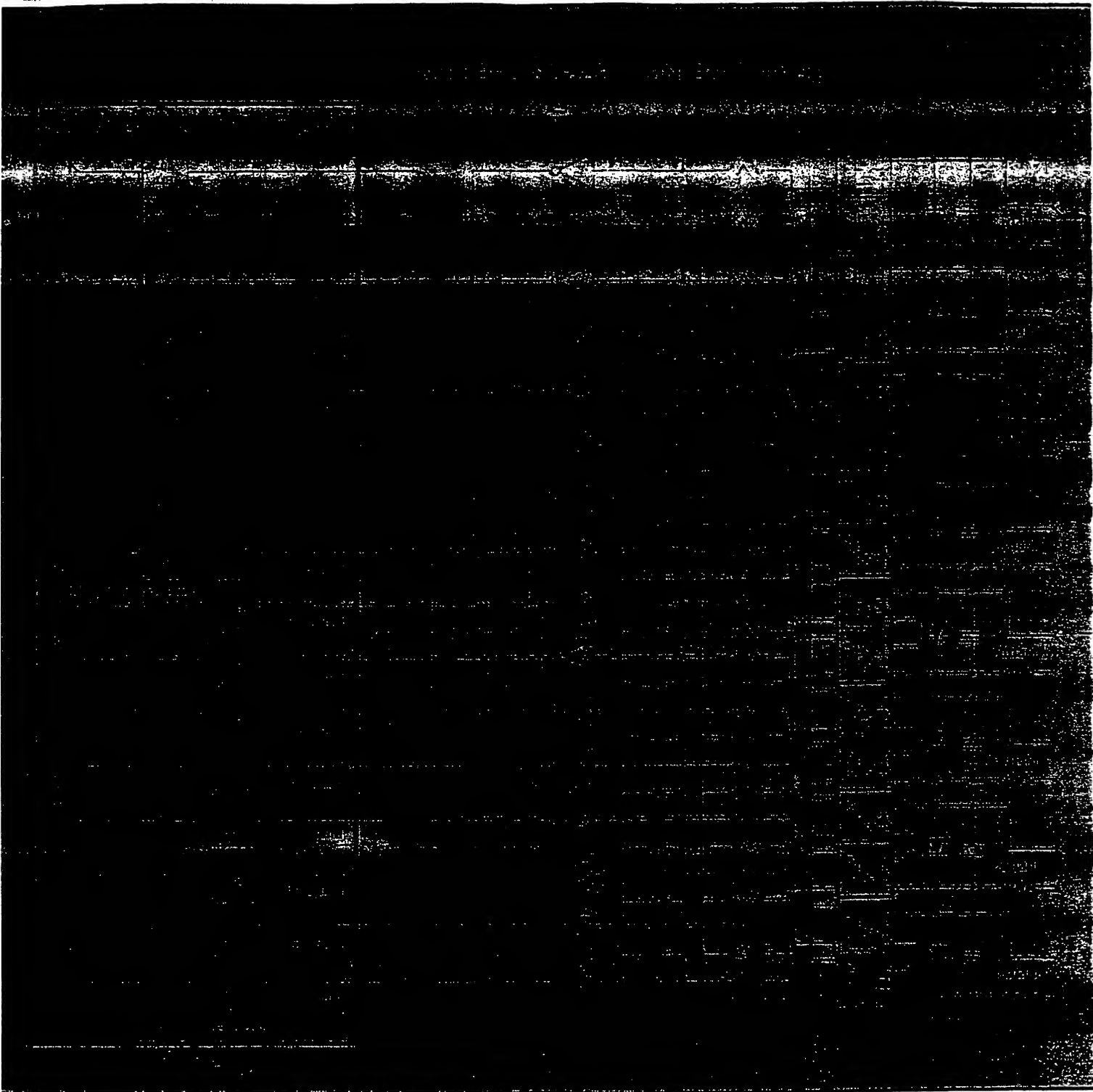
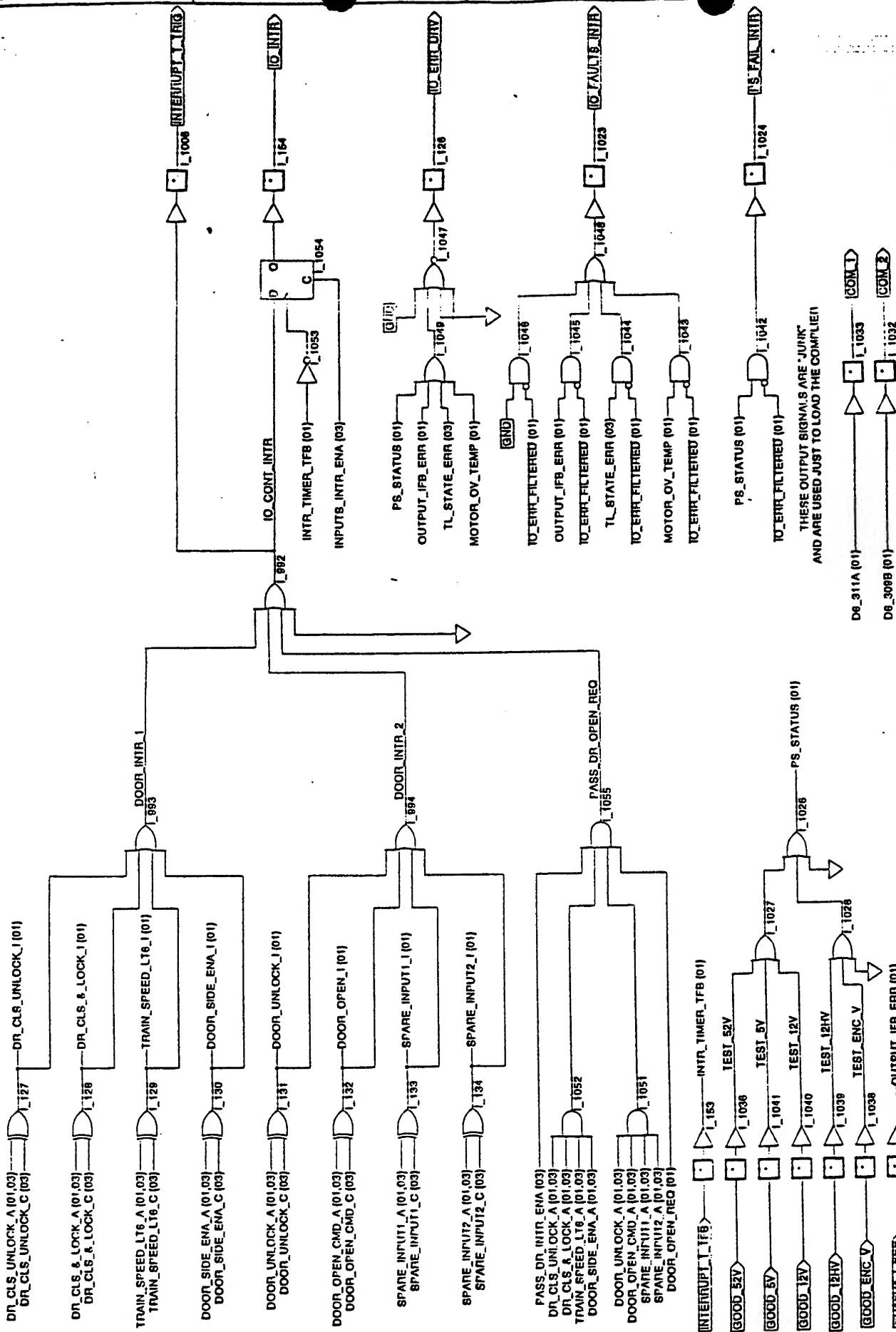


FIGURE 11

↑
310

INTERRUPT AND FILTER CONTROL CIRCUITS



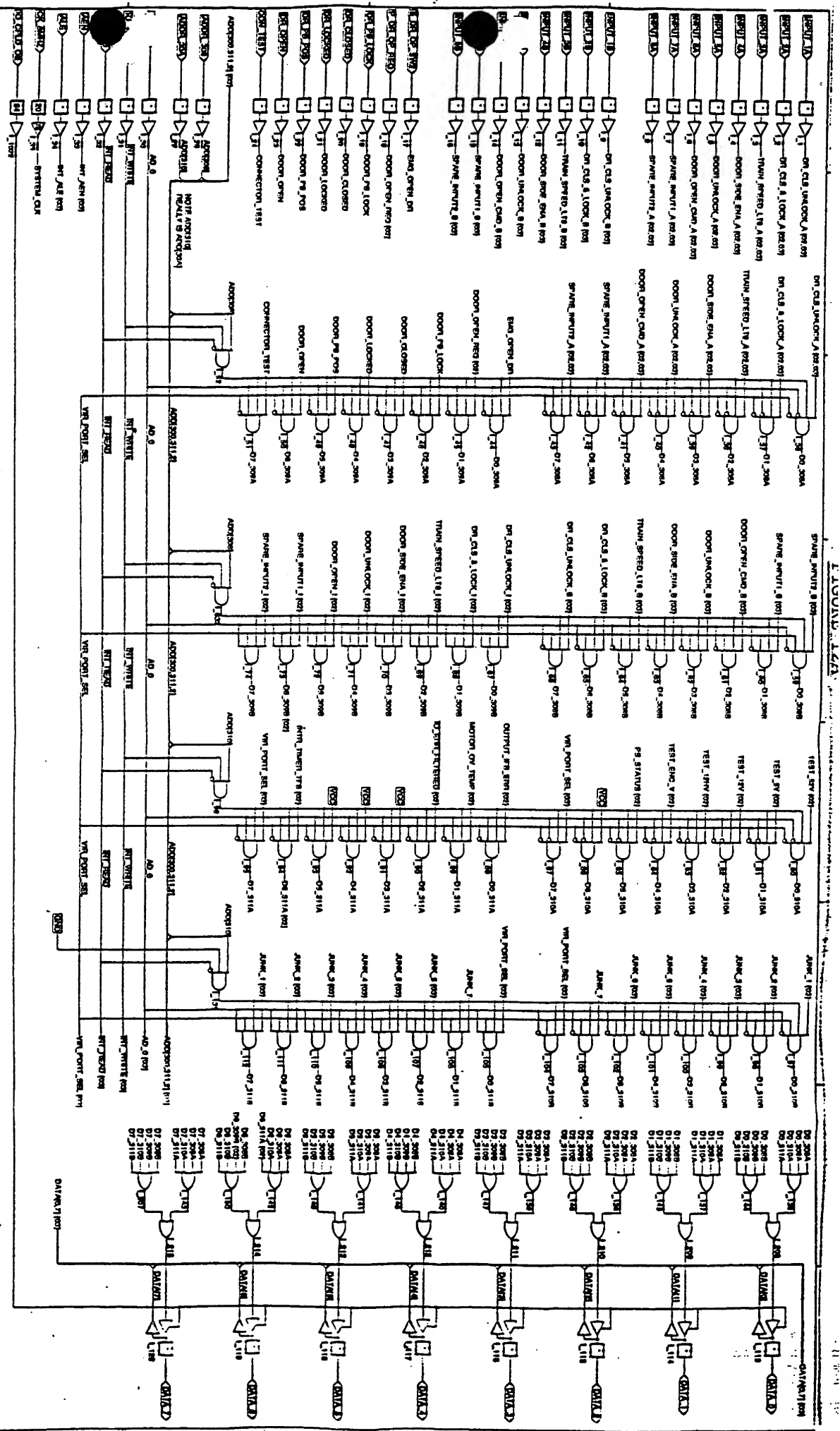
MD-I/O CARD
(I/O-CPU0 INTERRUPT AND
FILTER CONTROL CIRCUITS)

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FIGURE 12C

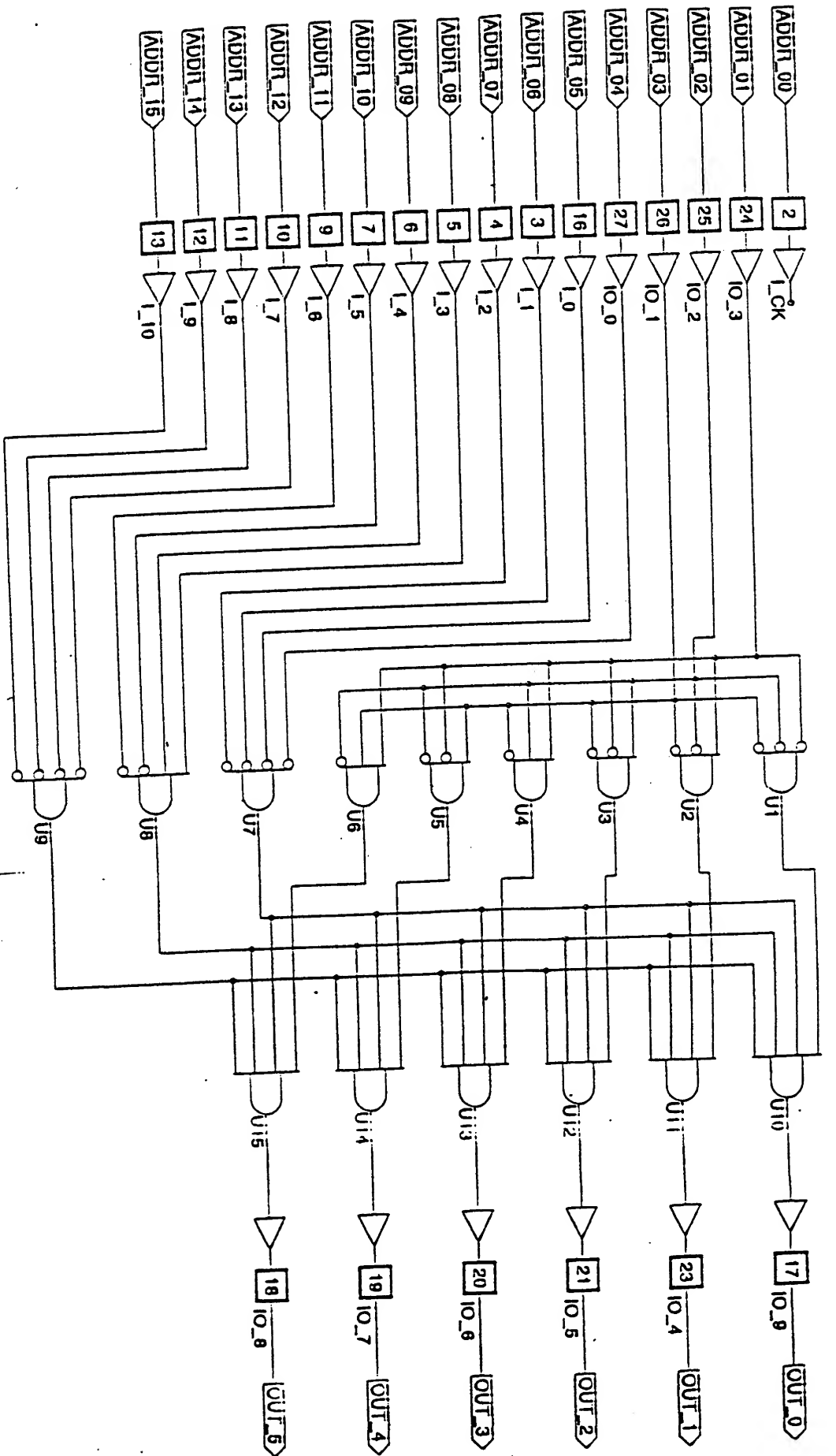
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MD-140 CARD
 (I/O-CARD DATA/ADDRESS)
 CONTROL LOGIC



FIGURE 13



MD-I/O CARD
(Add-CPLD Logic)

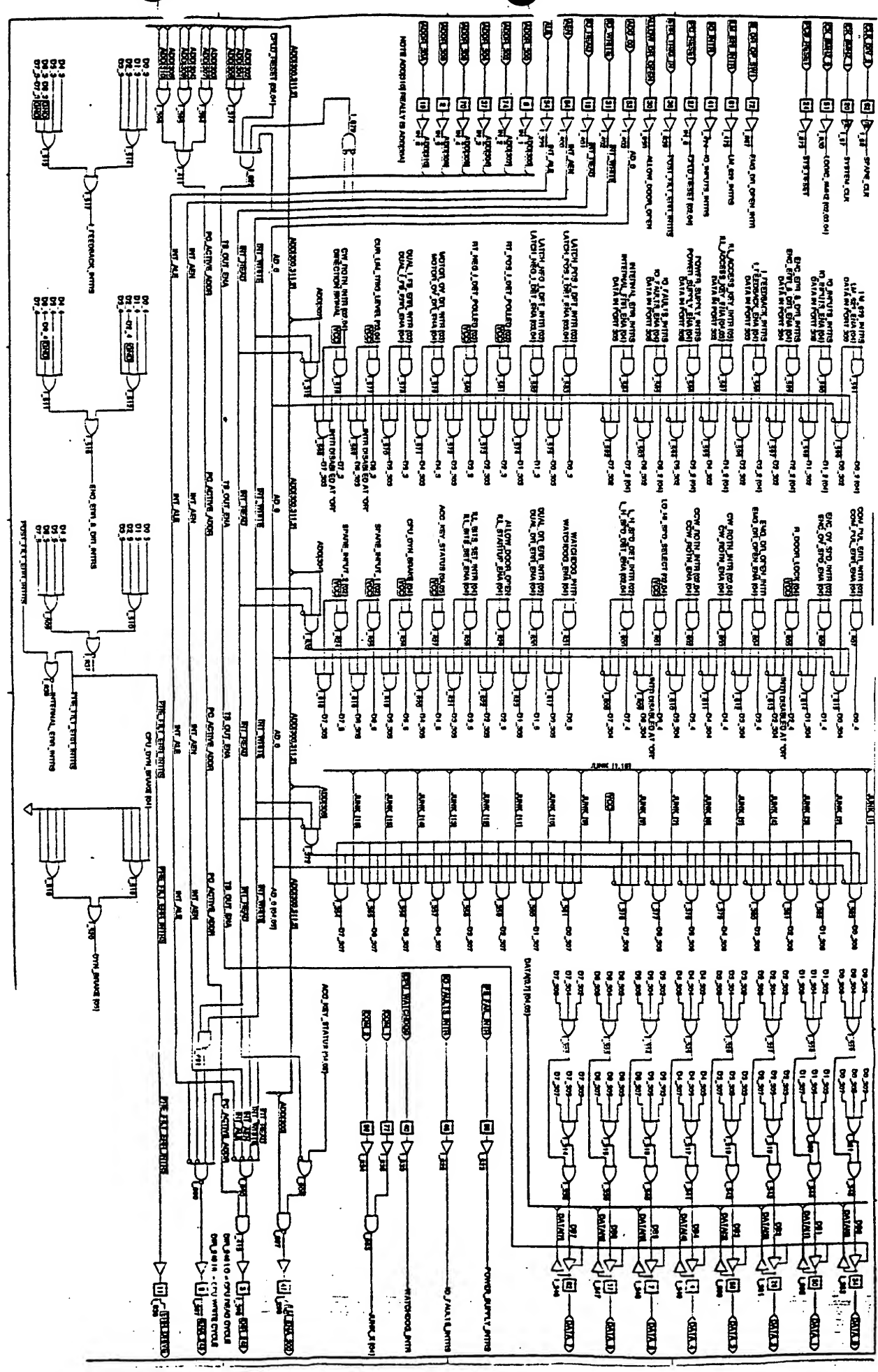


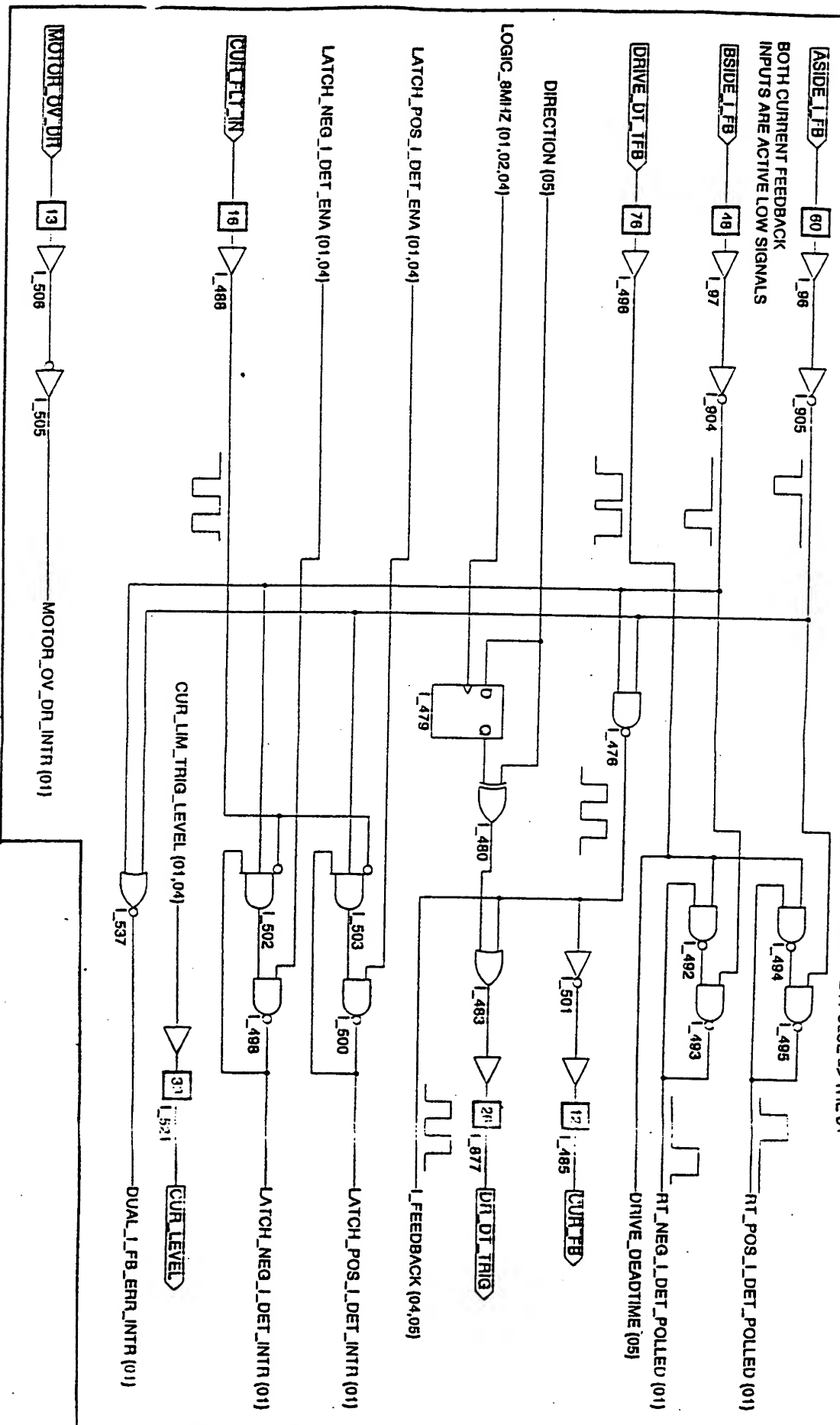
FIGURE 14A

MD-1/0 CARD
(Mc-CPLD DATA/ADDRESS)
CONTROL LOGIC

FIGURE 14B

CURRENT FEEDBACK & DEADTIME CIRCUITS

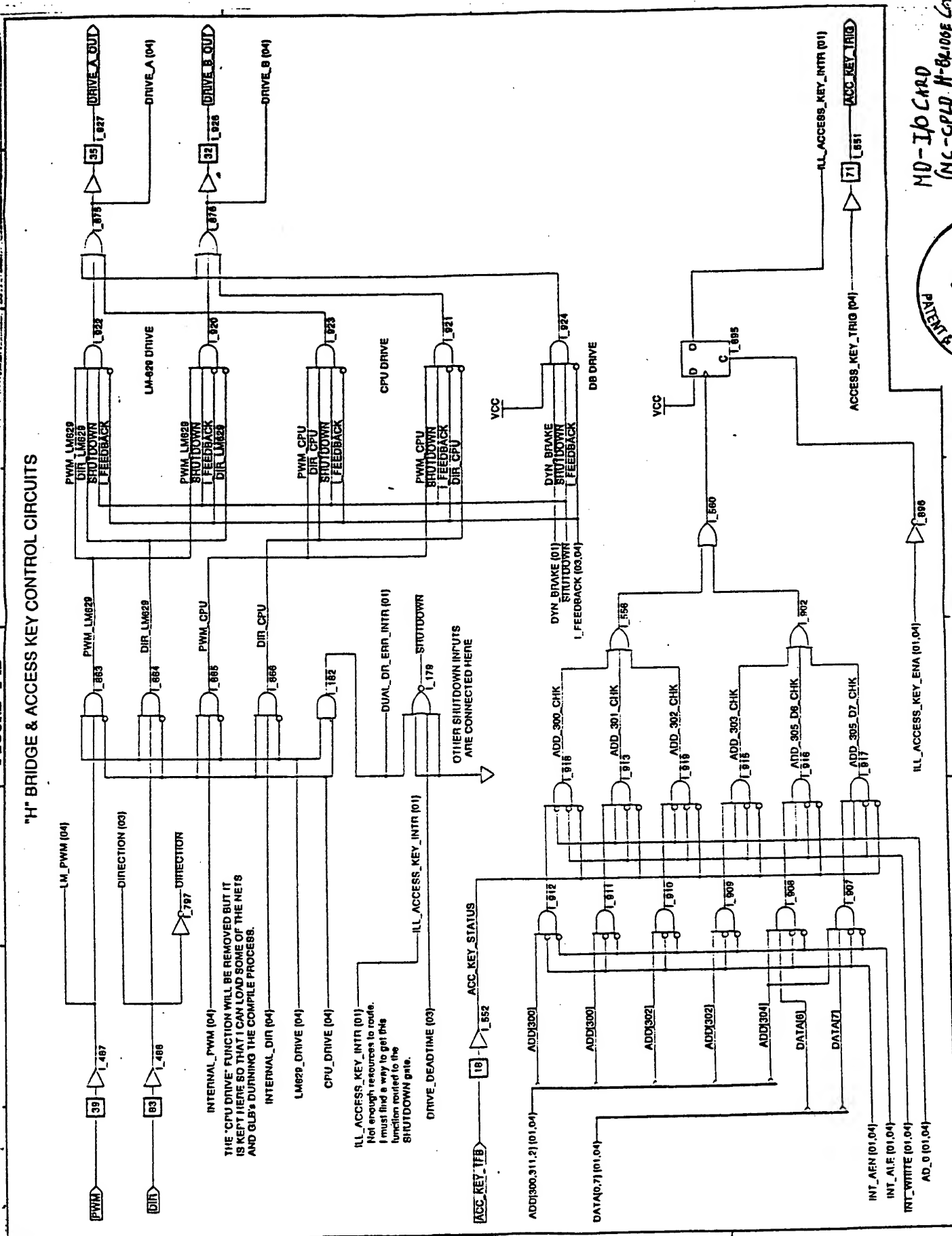
THIS IS A CURRENT PULSE STRETCHER CIRCUIT THAT WILL ALLOW THE I PULSE => THE DI



MD-I/O CARD
(MC-CPLD CURRENT FEEDBACK
AND DEADTIME CIRCUITS)

FIGURE 14D

"H" BRIDGE & ACCESS KEY CONTROL CIRCUITS

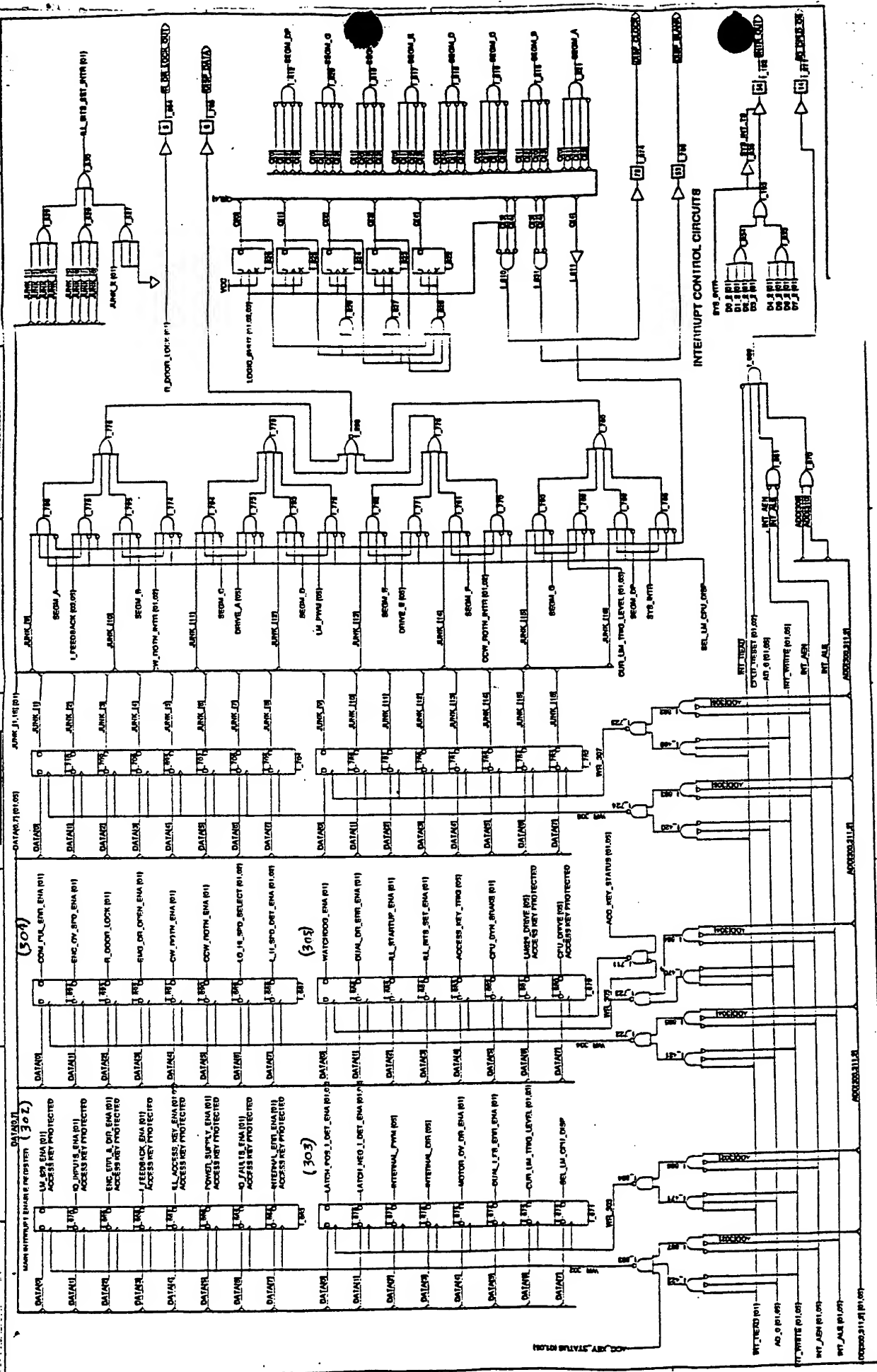


MD-IP CARD
(MC-CPLD, H-Bridge Control)
(AND Access Key Control)

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FIGURE 14E.



MD-IB CARD
(MC-CPLD INTERRUPT)
(CONTRAL LOGIC)



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